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STATISTICAL STATIC TIMING ANALYSIS OF CMOS CIRCUIT USING PATH BASED ANALYSIS

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ABSTRACT
In the field of high-speed technology applications, the three most challenging objectives for design engineers are the high performance of the circuit, low power, and small area consumption on the chip. The proposed work implements Statistical Static Timing Analysis using Path-based analysis. The implemented statistical algorithm uses 32nm technology. Parameter Space and performance space are the two parts of the algorithm. The parameter space deals with a statistical MOSFET model whose drain current and gate capacitance are the functions of process and environment parameters. Whereas, the performance space relates to the statistical library of logic gates. To validate the results, we compared the results with software-based simulation analysis and better results are confirmed. It is observed that the use of the proposed approach of SSTA, took less time to produce similar results. Hence, we claim that SSTA will be helpful to control the variation in MOSFET parameters like length, width, oxide layer thickness, and threshold voltage.

KEYWORDS:
Static Timing analysis, Process Variations

INTRODUCTION

Timing analysis is one of the important specifications in high speed Very Large Scale Integration (VLSI). Timing analysis is used to determine the operating clock frequency of the digital circuit. The reciprocal of the lengthiest path delay between the input and output of the VLSI circuits is the operating frequency of the circuit. One of the most popular methods to calculate the operating frequency of the VLSI circuits is Static Timing Analysis (STA). The word "Static" points out to the fact that the timing analysis is carried out in an input-independent manner, and asserts to find the worst-case delay of the circuit over all possible input combinations.
As deep submicron semiconductor technology moves on the nanometer regime, there is increasing relative uncertainty in process parameters. This variation in process parameters can also be categorized into two types of variables, i.e. Inter-die variations and Intra-die variations [1] [2]. Inter-die variations are the variations from one die to other die, one wafer to another and one slot of the wafer to another slot of the wafer as shown in Fig. 1.

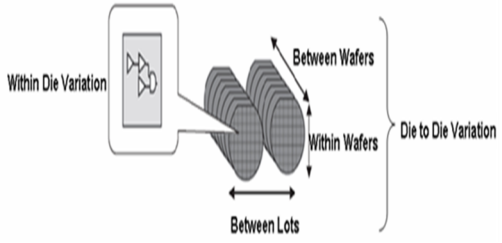

Fig. 1. Within die and die to die variation

Inter dies variations are affect all the MOSFETs on the same chip in the same manner, e.g., they may affect all the MOSFET gate width of the devices on the one chip to be bigger or all of them to be minor. On the other hand, Intra-die variations are the variations within a single chip, and may affect different MOSFETs on the

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same chip, e.g., they may result in some MOSFET having a minor length than the normal, while others may have greater.

OBJECTIVES

The main goal of this project work is, to calculate the accurate operating frequency of the CMOS circuit for high speed technology applications by considering the process parameter variations like length, width, oxide thickness, and dopant of the MOSFET and environment variations like temperature and power supply variation. We have applied our algorithm using path based analysis on specific digital circuits like Demultiplexer and Decoder. To apply data structure algorithm over a graph, a circuit is expressed by a graph that represents the gates and interconnects as nodes. Traversing the graph, the Probability Density Function of the delay in each node is calculated using the statistical sum and max operation with the delay variations of the gates and interconnects as inputs. The delay of the entire circuit can be analyzed by using statistical max operation while traversing the graph.

METHODOLOGY

Fig. 2 shows the basic flow of the Statistical Static Timing Analysis algorithm. The algorithm is divided into two parts i.e. Parameter Space and Performance Space. In Parameter space we developed a statistical MOSFET model whose drain current and gate capacitance are the functions of process parameters and environmental parameters [3]. In the Performance Space, we developed the statistical library of logic gates. Using this library, we apply path-based analysis on various combinational.

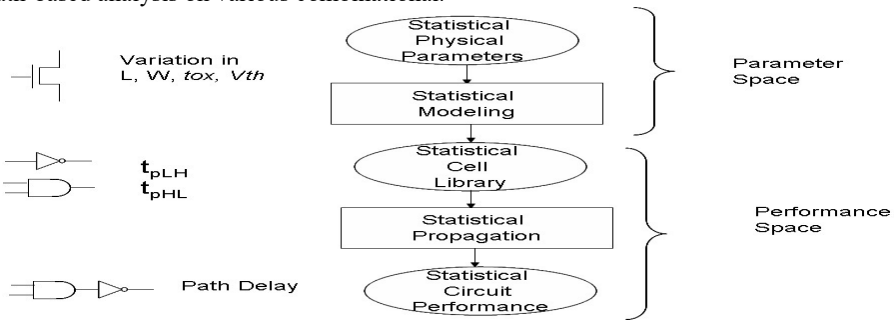

Fig. 2. The Basic flow of the SSTA Algorithm

The concept, "the propagation delay of a logic gate is dependent on the driving capability of the driving gate and input capacitance of the load gate" is explained in [3]. The driving or drain current of a MOSFET is the function of channel dimensions. It is directly proportional to the width and inversely proportional to the length of the channel. Thus, change in length or width of the channel causes change in the drain current. It also changes the propagation delay of logic gates. Similarly, the gate capacitance of the MOSFET is directly proportional to the area of the gate and inversely proportional to the oxide thickness. In the nanometer regime, all these parameters can vary randomly. It produces a difficulty to calculate accurate propagation delay. "The statistical analysis is one of the best solutions to calculate drain current and gate capacitance" [3].

We implemented the statistical MOSFET model of [3]. It is found that it can calculate the drain current with accuracy. The gate capacitance is also obtained accurately. WE followed the following algorithm. We kept all parameters constant except one to get the value of drain current and gate capacitance. Thus the effect of that particular parameter can be studied with better accuracy. The algorithm considers parameters like length, width, temperature, dopant concentration, oxide thickness and supply voltage, recursively.

DESIGN DESCRIPTION

Modeling of 4:1 Multiplexer: A multiplexer is a combinational logic circuit with many inputs and single output. The select input lines decides which input is to be connected to the output. If there are n selection lines, then the number of maximum possible input lines is two to the power n. The multiplexer is always preferable over a logic gate circuit in large circuit design, since the multiplexer generates, a small number of glitches than the circuit using the logic gate. By considering this most important advantage of multiplexer we design the 4:1 multiplexer circuit as shown in Fig. 4. The input combinations 11, 10, 01, and 00 on the select lines switch I_3, I_2, I_1 and I_0 to the output respectively. In the Boolean expression in equation (1) Y represents the output.

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$$Y = I_0 \cdot \overline{S_1} \cdot \overline{S_0} + I_1 \cdot \overline{S_1} \cdot S_0 + I_2 \cdot S_1 \cdot \overline{S_0} + I_3 \cdot S_1 \cdot S_0 \quad (1)$$

The path delay of MUX is the summation of the propagation delay of the AND gate and the propagation delay of the OR gate. The propagation delay is the function of output resistance of the gate and load capacitance of the gate. The value of resistance and capacitance depends on the process parameters of MOSFET and environmental parameters [3].

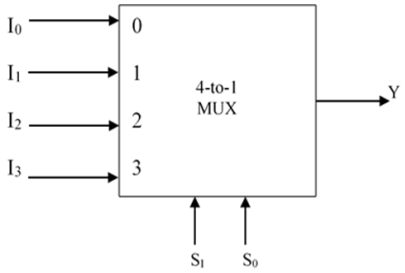

Fig. 3. Block Diagram of 4:1 Multiplexer

The operating frequency of the MUX can be decided by calculating the path delay of the circuit. In this 4:1 multiplexer total 4 paths are from input to output. The circuit diagram shown in Fig. 4 is converted in the form of a graph. To calculate accurate delay of the circuit, we used Path based analysis. In Path based analysis the propagation delay of logic circuit can be traversing the graph path by path. One of the path, i.e. from input I0 to Y of the MUX is shown in Fig.5.

The delay of each path is calculated by considering the delay of each node [4]. The graph shown in Fig. 6 has three different paths. The Path 1, Path 2 and Path 3 delays is given by equation (2), (3), and (4) respectively. The worst case delay out of three can decide the operating frequency of the logic circuit.

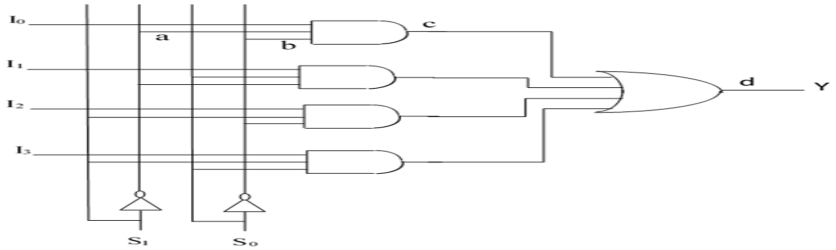

Fig. 4. Logic diagram of 4:1 Multiplexer

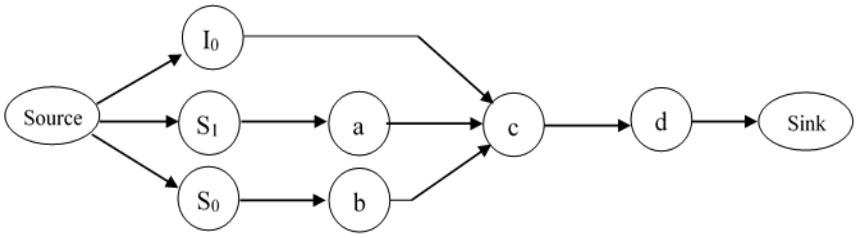

Fig. 5. Graph for path I0 to Y of MUX

DP1 = td (I0...c) + td (c..d) (2)
DP2 = td(S1..a) + td (a..c) + td (c..d) (3)
DP3 = td(S0..b) + td (b..c) + td(c..d) (4)

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Modeling of 2:4 Decoder: The path delay of the decoder is the summation of the propagation delay of AND gate and the propagation delay of NOT gate [5]. The propagation delay of both the gates is the function of output resistance of the gate and load capacitance of the gate. These resistance value and capacitance value depends on the process parameters of MOSFET and environmental parameter. We applied the proposed algorithm on a 2:4 decoder of Fig. 7 and do the analysis. The designed decoder uses the logic gates. The logical diagram is as shown in Fig. 6. The Boolean equations for each output are given from equation (5) to (8).

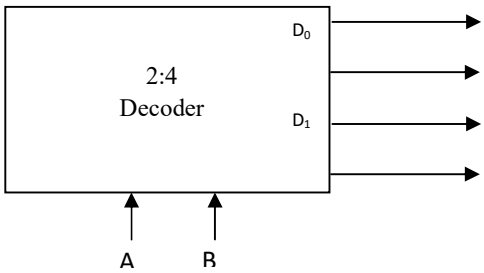

Fig. 6. 2:4 decoder

$$D0 = S1 \cdot S0 \quad (5)$$

$$D1 = S1 \cdot S0 \quad (6)$$

$$D2 = S1 \cdot S0 \quad (7)$$

$$D3 = S1 \cdot S0 \quad (8)$$

The path delay of Decoder is the summation of the propagation delay of AND gate and propagation delay of the NOT gate. The propagation delay of NOT gate is the function of output resistance NOT gate and the load capacitance of the AND gates [3]. Similarly, the propagation delay of the AND gate is the function of the output resistance of the AND gate and the load capacitance of the gate connected to the out terminal of the decoder. These output resistance values and load capacitance value are depended on the process parameters of MOSFET and environmental parameter and since these parameters are not fixed so the propagation delay can vary according to the variations in these parameters.
The operating frequency of the Decoder can be decided by calculating input to output path delay of the logical circuit shown in Fig. 8. In this 2:4 Decoder has a total of 8 paths from input to output. For path-based statistical timing analysis, we transfer the logical diagram into its equivalent graph shown in Fig. 9.

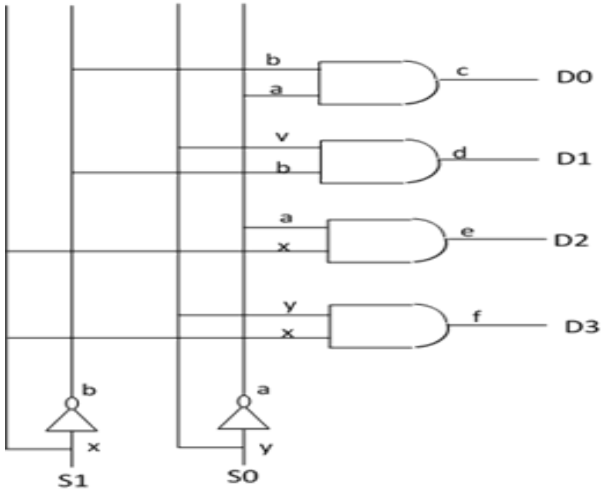

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Fig. 7. Logic diagram of 2:4 Decoder

Fig. 9 shows the weighted graph for 2:4 decoder. The weight of each edge is the propagation delay of the logic gate. For calculation purposes we assume the propagation delay of NOT gate 1 time unit and the propagation delay of AND gate is 2 time units [6].

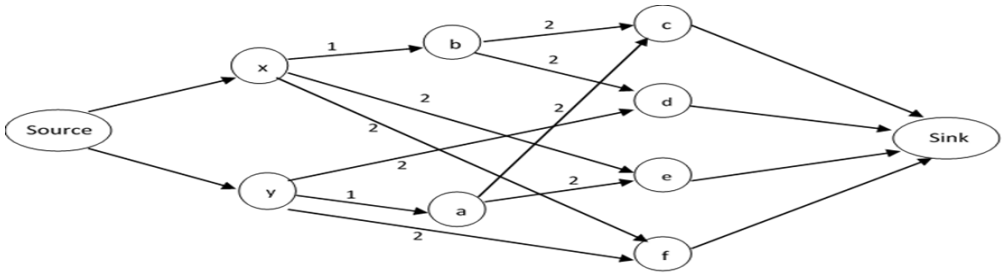

Fig. 8. Graph for 2:4 Decoder

SOFTWARE

We implemented our proposed system using the MATLAB programming language. The input to this system is variation in effective channel length, the oxide thickness, the dopant concentration, and the transistor width and the output is variation in drain current (which drives the load capacitance) and gate capacitance of MOSFET which acts as a load capacitor on the driving gate.

We discussed the simulation of the cell library for the logic gates. Using these library cells, we designed and simulate various MSI digital circuits. We start our simulation with SSI circuit, i.e. NOT, NAND, NOR, AND, OR gates. Then we also implemented MSI circuits i.e. the Multiplexer and Decoder. Both these models developed using NOT gates, AND gates and OR gates. The user-defined functions of all these cells are already designed and simulated with us. We integrate these functions of the logic gates to simulate the functionality of the multiplexers and decoders shown below.

User define function for 4:1 Multiplexer:

```
tpand=AND2in;
tpor=OR2in;
tpnot=Notgate;
tp=tpnot+2*tpand+2*tpor;
```

User define function for 2:4 Decoder:

```
tp=AND2in;
tpnot=Notgate;
tp=tp+tpnot;
```

SIMULATION RESULTS AND DISCUSSION

The statistical delay of the combinational logic circuit is calculated statistically and using Monte Carlo analysis. Fig. 10 shows the propagation delay distribution of 4:1 multiplexer. It is observed from the figure that all the statistical propagational delay distributions closely matching with the Monte-Carlo simulation result. The error between the statistical and Monte Carlo analysis are given in Table 1. The result in the table shows that the simulation time for the proposed analysis is less by 23.34% compared to the Monte Carlo analysis.

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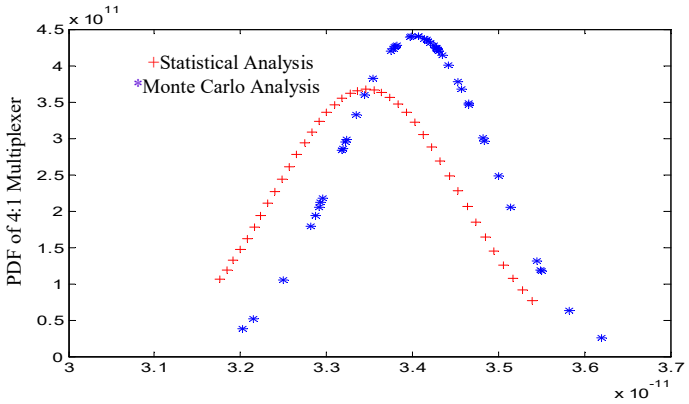

Fig. 9. PDF of 4:1 Multiplexer

Statistical analysis			Monte Carlo analysis			% Error	
Mean (ps)	***Standard Deviation (ps)***	***Simulation Time (s)***	***Mean (ps)***	***Standard Deviation (ps)***	***Simulation Time (s)***	***Mean***	***Standard Deviation***
33.469	1.0858	4.026	34.030	0.90586	5.252	1.64	19.86

TABLE I. Comparison of Statistical Delay Analysis and Monte Carlo Analysis for 4:1 Multiplexer

The statistical delay of 2:4 decoder is calculated using statistical analysis and Monte Carlo analysis. For a considerable accuracy in the analysis, we run our algorithm around 1000 iterations for Monte Carlo simulation. Fig. 11 shows the propagation delay distribution of 2:4 decoder. It can be observed from the figure that the statistical propagation delay distributions are closely matching with the Monte-Carlo simulation result.

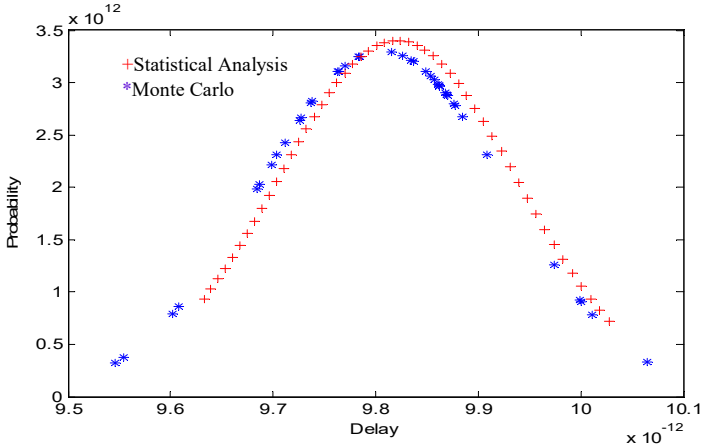

Fig. 11. PDF of 2:4 Decoder

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The error between statistical and Monte Carlo analysis is 0.15% for mean and 2.9% for standard deviation given in Table 2. The result in the table shows that the simulation time for the proposed analysis is less by 27.19% compared to the Monte Carlo analysis.

Statistical analysis			Monte Carlo analysis			% Error	
Mean (ps)	Standard Deviation (ps)	Simulation Time (s)	Mean (ps)	Standard Deviation (ps)	Simulation Time (s)	Mean	Standard Deviation
9.8210	0.11727	3.173	9.8062	0.12078	4.358	0.15	2.9

TABLE II. Error of Statistical Analysis against Monte Carlo Analysis for 2:4 Decoder

CONCLUSION

We studied Statistical Static Timing analysis for high-speed technology applications. The objective of the work was to calculate the accurate operating frequency of the logic circuits by considering the process parameter and environmental parameter variations. We considered four process parameter variations i.e. length, width, oxide thickness, and dopant of the MOSFET and two environmental parameter variations like Temperature and Supply Voltage variation. In this paper, we proposed a statistical static timing analysis of 4:1 multiplexer and 2:4 decoder using Path-based analysis. We found that the percentage error between proposed SSTA and Monto-Carlo analysis is 1.64% and 19.86% for mean and standard deviation respectively for 4:1 multiplexer while 0.15 and 2.9 mean and standard deviation for 2:4 decoder. The percentage error for mean and standard deviation is below 25% which is quite less.

Type of Module	Percentage Errors in Path-Based Analysis	
	Mean	***Standard Deviation***
Multiplexer	1.64	19.86
Decoder	0.15	2.9

Table III. Percentage Errors in Path-Based Analysis

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