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Design and Simulation of 2:1 Multiplexer For Low Power and Minimum Area

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ABSTRACT
Multiplexer (MUX) is most significant segment of correspondence framework. Multiplexer is utilized to raise the productivity of information transmission. Likewise multiplexer is utilized to use the more memory space of a PC in a successful manner. It convert parallel to serial data in transmission systems. Multiplexer is otherwise called a "MUX". Multiplexer is the place information must be changed from various sources to a goal. In VLSI research region force and territory of the structure is decreased. The standard cell based, semi – custom and full custom design methodologies are utilized to structure multiplexer. These techniques decrease the size, zone and force utilization multiplexer. 45 nm technology is utilized to assess the work. These plan strategies are dissected and advance territory of multiplexer is purposed.

KEYWORDS:
CMOS, EDA tools, VLSI, NM Technology.

INTRODUCTION

The VLSI (Very Large Scale Integration) is significant device, used to integrate the number of components on single chip. The significant components are region decrease and least force utilization. Presently days, the interest for zone decrease and force factors are expanding. Different plan methods are produced for increment the presentation of circuits. The high temperature impacts in silicon disappointment. Consequently circuit will be harmed.

Another factor power consumption is reduce electricity consumption. Multiplexer is very important in telecommunication industry. Also multiplexer is key component of any arithmetic circuit. In a communication system, Multiplexer is used to transmit the signals in between transmitter and receiver.

The important function of multiplexer is to take n number of input and lines and gives one output line. The demultiplexer is, inverse to the operation of the multiplexer. The main function of the Multiplexer is convert parallel to serial data line. Figure 1 shows multiplexer and demultiplexer for data transmission.

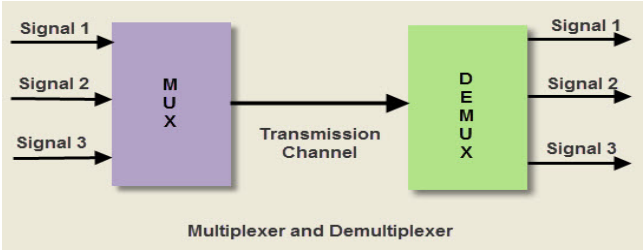

Figure 1: Transmission using mux and demux

PROPOSED METHODOLOGY

CMOS circuit requires exceptionally low force for activity. The static CMOS circuit is appeared in Figure 2. CMOS innovation is generally utilized in the structuring of the VLSI circuits

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PROPOSED MULTIPLEXER USING CMOS: MOS transistor have two sorts are NMOS and the PMOS. NMOS transistor can gives strong "0" and weak "1" and PMOS transistor gives strong "1" and weak "0". In the wake of consolidating PMOS and NMOS transistors CMOS transistor is shaped. When contrasted with the NMOS and bipolar transistors low force devoured by CMOS circuits. Standard cell based, semi-custom and full custom are the structure approaches used to configuration IC's. This paper depends on the area efficient 2:1 multiplexer utilizing microwind instrument. Figure 3 shows the schematic graph of 2:1 MUX. General NAND entryway structured utilizing CMOS gate.7 PMOS and 7 NMOS transistors are utilized to plan NAND gate. PMOS transistor is associated with the Vdd to the yield and NMOS is associated with the yield to Vss. In this CMOS transistor PMOS transistor is function as pull up resistor and NMOS transistor fill in as pull down resistor.

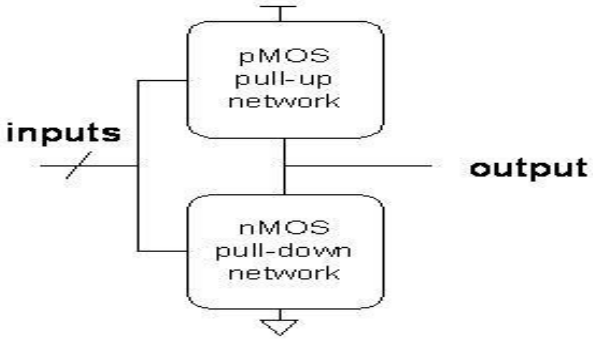

Figure 2: Static CMOS Circuit

HARDWARE AND SOFTWARE IMPLEMENTATION DETAILS

The Microwind tool is utilized to design as well as simulate 2:1 Multiplexer. The figure 3 shows schematic of 2:1 multiplexer utilizing NAND gates. To design CMOS gate PMOS and NMOS gates are required. Figure 4 shows the layout of standard cell based design. This design required more area and consumed more power.

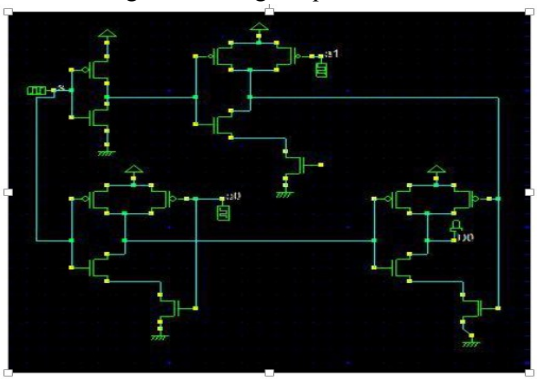

Figure 3: Schematic of 2 to 1 multiplexer using NAND gates

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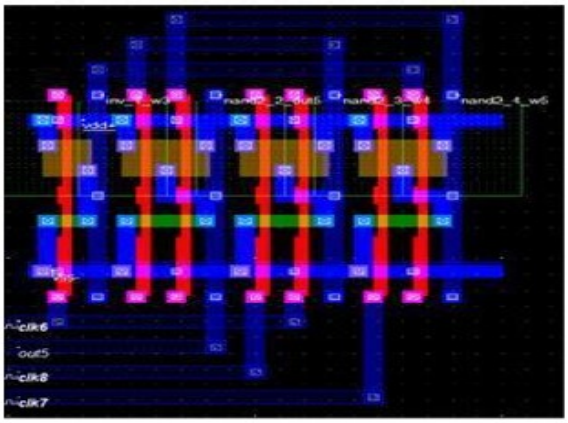

Figure 4: Standard cell based layout

Figure 5 shows the layout of Semi-custom design

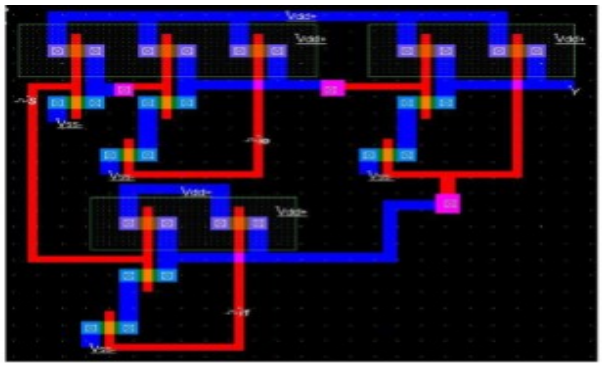

Figure 5: Semi-custom design

Figure 6 shows the full custom design.

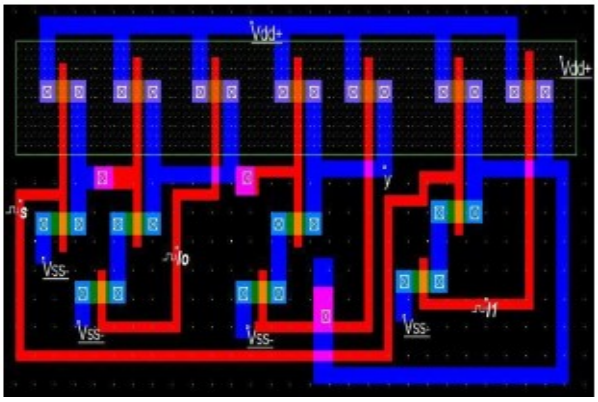

Figure 6:Full custom design

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RESULTS AND DISCUSSION

The main parameters area and Power consumption of the 2 to 1 multiplexer in this paper are consider. Table 1 shows the area and power consumption by 2 to 1 multiplexer circuit.

Table1: Area and Power consideration

Multiplexer Layout	Technology Used	Area	Power Consumption
Standard Cell Based Design	45nm	3.20 pm^2	0.963µW
Semi-Custom Design	45nm	1.81pm^2	0.655µW
Full Custom Design	45nm	1.55pm^2	0.368 mW

Technology used to design standard cell based layout, semi-custom based layout and full custom layout is 45nm technology.

CONCLUSION

We designed and simulate three distinctive sort design of 2 to 1 multiplexer. Standard cell based design, semicustom based design and full custom design are produced for the 2 to 1 multiplexer utilizing microwind. As far as intricacy, semi-custom format and full custom design is less intricate than standard cell based design. Power utilization and area of the full custom layout design is less than semicustom based layout design and standard cell based.

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